

IN THE SPECIFICATION

Please amend paragraph [0057] of the present application as follows:

TP [0057] FIG. 8 shows logic 800 that is one embodiment of logic 510 ^{5A} ~~[[500]]~~ of FIG. 5 for controlling a row of memory cells in array 210. Logic 800 includes NAND gates 801-803, AND gate 804, NOR gates 805-807, OR gate 808, inverters 810-814, and inputs to receive a data bit DIN, a write enable signal WR_EN, a power-on reset signal POR, a pre-charge signal PCH, a pre-discharge signal PDCH, a test signal TEST, and the write control signal WR. In response to DIN and the control signals, logic 800 generates the dataline control signals ch_dl, dch_dl, ch_dlb, and dch_dlb and the dataline driver control signals \overline{RD} and WR.

during read operations. For example, FIG. 12 shows a dataline driver 1200 that is another embodiment of dataline driver 214. Dataline driver 1200 is similar to dataline driver 214, with the addition of PMOS transistors 1201-1202, NAND gates 1203-1204, and inverters 1205-1206. PMOS transistor 1201 is coupled between V_{DD} and DL(1) and has a gate coupled to the output of NAND gate 1203, which includes a first input coupled to DL(2) and a second input to receive \overline{RD} via inverter 1205. Together, PMOS transistor 1201 and NAND gate 1203 allow a logic high signal on DL(2) to propagate to DL(1) during read operations. Similarly, PMOS transistor 1202 is coupled between V_{DD} and DL(1) and has a gate coupled to the output of NAND gate 1204, which includes a first input coupled to DL(2) and a second input to receive \overline{RD} via inverter 1206. Together, PMOS transistor 1202 and NAND gate 1204 allow a logic high signal on DL(2) to propagate to DL(1) during read operations.

[0056] Accordingly, for embodiments that utilize the dataline driver 1200 of FIG. 12, the PMOS pull-up transistors MP1 and MP2 in memory cells 400 may be tested in the manner described above for testing the NMOS pull-down transistors MN1 and MN2, thereby eliminating steps 702-704 and 709-711 which, in turn, reduces testing time. However, although allowing for faster testing of PMOS transistors MP1 and MP2, dataline driver 1200 occupies more silicon area than dataline driver 214.

TP [0057] FIG. 8 shows logic 800 that is one embodiment of logic 510 of FIG. 5A for controlling a row of memory cells in array 210. Logic 800 includes NAND gates 801-803, AND gate 804, NOR gates 805-807, OR gate 808, inverters 810-814, and inputs to receive a data bit DIN, a write enable signal WR_EN, a power-on reset signal POR, a pre-charge signal PCH, a pre-discharge signal PDCH, a test signal TEST, and the write control signal WR. In response to DIN and the control signals, logic 800 generates the dataline control signals ch_dl, dch_dl, ch_dlb, and dch_dlb and the dataline driver control signals \overline{RD} and WR.